

U.S. PATENT & TRADEMARK OFFICE
NOV 28 2003

SUPPLEMENTAL DECLARATION AND POWER OF ATTORNEY FOR REISSUE PATENT APPLICATION

Attorney Docket No.
018760-016

As the below-named inventors, we hereby declare that:

Our residence, post office address and citizenship are as stated below next to our names;

We believe we are the original, first and joint inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR ELEMENT MODULE AND SEMICONDUCTOR DEVICE WHICH PREVENTS SHORT CIRCUITING

the specification of which is attached hereto;

We have reviewed and understand the contents of the above-identified specification, including the claims;

We acknowledge the duty to disclose all information known to us to be material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56;

We believe the original patent is partly inoperative by reason of claiming less than we had a right to claim in the patent. One error which forms the basis for this belief is the fact that the patent discloses multiple concepts which underlie the invention, but the claims of the original patent are only directed to one of these concepts. Specifically, one of the aspects of the invention is the avoidance of capillary solder flow that results in short-circuiting of the leads of a semiconductor package, when the package is mounted so that it is in contact with a substrate. The features of the invention which pertain to this concept are reflected in the embodiments of Figures 2A-2B, 4A-4C and 5A-5B, for example.

Another aspect of the invention resides in the ability to mount a semiconductor package at a height which is lower than that which could be achieved with prior art devices. This problem is addressed in the patent at column 1, lines 56-61, and the solution provided by the invention is discussed at column 2, lines 13-17; column 4, lines 34-48; column 5, lines 24-36; and column 5, line 66 to column 6, line 4. This aspect of the invention is brought about by the features reflected in the embodiments of Figures 3A-3B and 6A-6B, for example.

The claims of the original patent are all directed to the avoidance of capillary flow. Each of claims 1, 5 and 7 recites "wherein said level difference serves to avoid capillary flow of solder . . ." Independent claims 3, 4 and 8 also recite that a claimed feature functions "to avoid capillary flow of solder." The failure to include claims which independently cover the features of the invention that provide the second aspect noted above, namely reduced mounting height, is an error which renders our patent partly inoperative in the protection of our entire invention.

All errors being corrected in this reissue application up to the time of filing this Declaration arose without any deceptive intention on our part.

We hereby claim foreign priority benefits under Title 35, United States Code Sec. 119 of the foreign application for patent as indicated below:

COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
Japan	9-315260	17 November 1997	YES <input checked="" type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>

**COMBINED DECLARATION AND POWER OF ATTORNEY
FOR REISSUE PATENT APPLICATION**

Attorney Docket No.
018760-016

We hereby appoint the attorneys and agent(s) associated with **Customer No. 21839**, including the specific individuals identified below, to prosecute said application and to transact all business in the Patent and Trademark office connected therewith:

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We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and believe are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	SIGNATURE	DATE
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